Bridged-Grain Metal-Induced Crystallization Poly-Si TFTs with Silicon Self-Implantation

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ABSTRACT

Silicon self-implantation is applied to passivate the defects in the grain boundaries of the metal-induced crystallization (MIC) poly-Si thin films. The material quality of MIC poly-Si thin film is improved. Bridged-grain (BG) thin film transistors (TFTs) fabricated on the resulting MIC poly-Si thin films exhibit improved device characteristics, including higher field-effect mobility, lower threshold voltage and higher on-off current ratio. The increased field-effect mobility is attributed to the reduction of the defect population in the grain boundaries of the MIC poly-Si thin film, thanks to the diffusion of the injected silicon interstitials into the grain boundaries.

1. Introduction

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) technology is one of the most promising candidates to realize high resolution active-matrix flat-panel displays, particularly those based on organic light-emitting diodes. The higher mobility of poly-Si TFTs than that of amorphous silicon (a-Si) TFTs allows higher aperture ratio when used as switching and driving transistors in the pixels and offers the possibility of integrating peripheral circuits with the pixel matrix, thus realizing a system on panel [1-3]. Compared to single-crystalline silicon transistors, poly-Si TFTs show poorer performance due to the existence of defective grain boundaries.

Much effort has been made to improve the quality of the poly-Si thin film, since it is one of the key factors that determine the performance of a TFT. The defect population will be reduced due to the passivation of defects in the grain boundaries. Hydrogen plasma is widely used as the passivation method by forming a Si-H bond [4, 5]. However, the thermal stability of Si-H bonds are poor, which will limit the process temperature in the TFT fabrication. Fluorine plasma and ion implantation are also investigated for the passivation of the grain boundaries trap states by forming Si-F bonds [6]. The advantages of the ion implantation method are easy control of dose and distribution of elements.

Silicon self-implantation has been studied to enlarge the grain size of poly-Si. High-dose silicon implantation at normal incidence is used to induce nearly full amorphization of the as-deposited poly-Si thin film, with only <110> seeds surviving as a result of the ion-channeling effect. The Si film was subsequently recrystallized, resulting in large grain size due to low seed density [7]. TFTs based on such Si-implanted and recrystallized poly-Si film demonstrated increased mobility [8]. However, this method has the issue of the high ion implantation dosage and non-uniformity of the poly-Si film. Recently oxidation-induced injection of Si interstitial has been adopted to improve the performance of TFTs fabricated on MIC poly-Si [9]. The oxidation takes place during the crystallization by replacing the commonly used N_2 with O_2 in the annealing atmosphere.

The implantation of Si is an alternative and more precise technique of introducing Si interstitials. In this paper, the effects of Si implantation, particularly their dose dependence, are studied by monitoring the change in the field-effect mobility of TFTs fabricated on Si-implanted poly-Si thin films. These findings are consistent with the mechanism of increased mobility attributed to O_2 annealing.

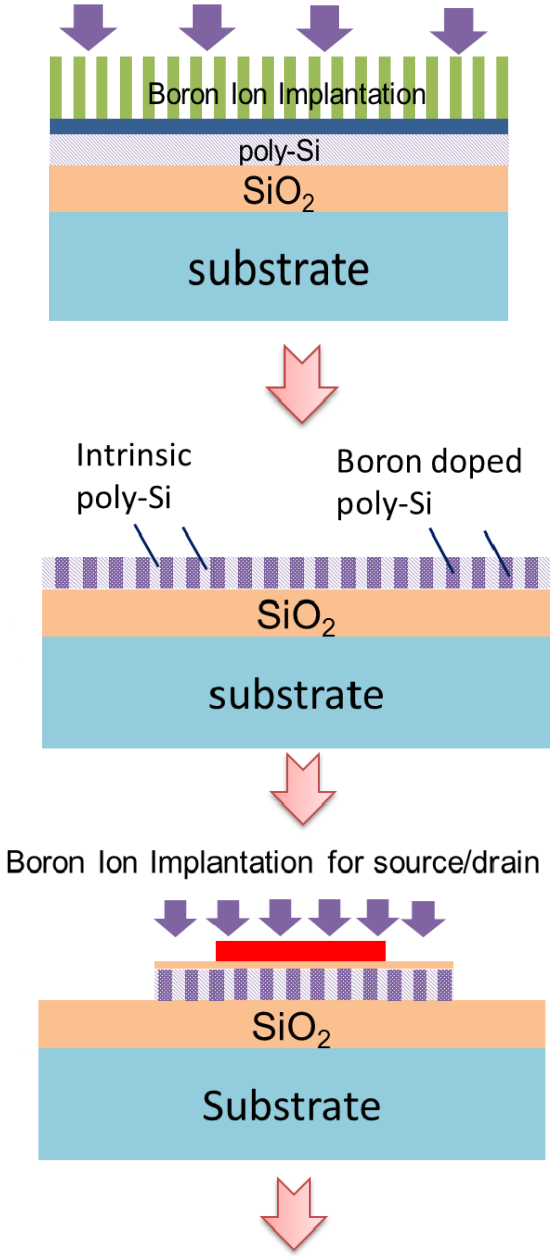
2. Device Fabrication

The fabrication process began with 100 mm sized silicon wafers covered with 500-nm thick thermal oxide. Amorphous silicon (a-Si) thin film was deposited as active layer by low-pressure chemical vapor deposition (LPCVD). In the MIC process, a thin layer of Ni/Si was sputtered on top of the a-Si layer using a Ni/Si target with a component ratio of Ni:Si=1:9. The substrate was then annealed at 600ºC for 10 hours in N_2. After annealing, the unreacted nickel was removed using a mixture of hot H_2SO_4 and H_2O_2. The poly-Si thin film were then implanted with silicon through 25-nm thick SiO_2 buffer layer at an energy of 15 keV and various doses ranging from 2×10^{14} to $8\times10^{14}/cm^2$. After implantation, the post-annealing process for implantation damage repair was carried out at 600 ºC in N_2 for 4 hours.

The poly-Si layer was then patterned to form the active islands using dry etching technique. After

removal of the native oxide on the surface of poly-Si layer using HF solution, 50-nm thick SiO_2 layer was deposited by LPCVD at 425 ºC as the gate dielectric. 300-nm thick Al was then sputtered and patterned as gate electrode using dry etch method. Self-aligned source and drain regions were implanted with boron at dose of 4×10^{15} /cm^2 and an energy of 20 keV. Then, 500-nm thick SiO_2 was deposited by LPCVD as the passivation layer before the contact holes were defined. 700-nm thick Al-1% Si was sputtered and patterned as probe pads.

Finally, the devices were sintered in forming gas for 30 min at 420 ºC. The key steps of the fabrication process are schematically shown in Fig. 1.



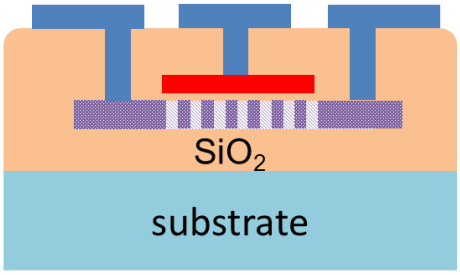


Fig.1 Key steps of the process flow of BG TFT fabrication

The dopants for the source/drain regions and the BG regions were activated simultaneously during the SiO_2 deposition by LPCVD and forming gas annealing process. The electrical properties of the MIC poly-Si TFTs were measured at room temperature using an HP 4156B semiconductor parameter analyzer. The respective channel length (L) and width (W) of the devices are 10 µm and 10 µm.

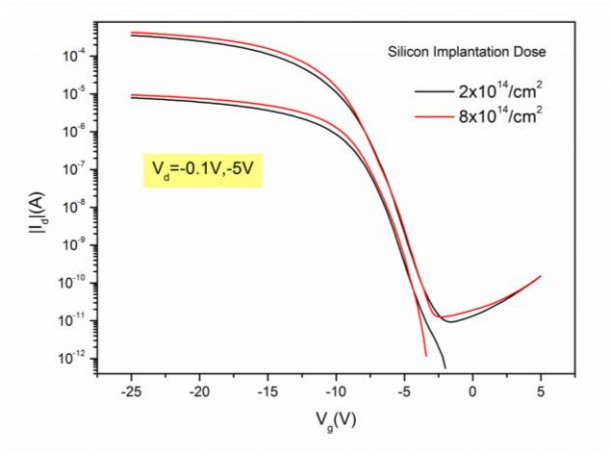
3. Results and Discussion

The comparison of the field effective mobility of the MIC TFTs with silicon self-implantation dose of 2×10^{14} and 8×10^{14}/cm^2 are shown in Fig.2. Twenty devices are measured for each sample. A clear trend of mobility increase is observed with increased Si implantation dose, as shown in Fig.3. For the electrical parameter, V_{th} is defined as V_{gs} when |Id| reached $W/L\times10^{-8}$ A at V_{ds}=-0.1 V, and the on-off current ratio is the ratio of maximum and minimum value of $|I_{ds}|$ at V_{ds}=-5V. The field effect mobility is estimated using the equation:

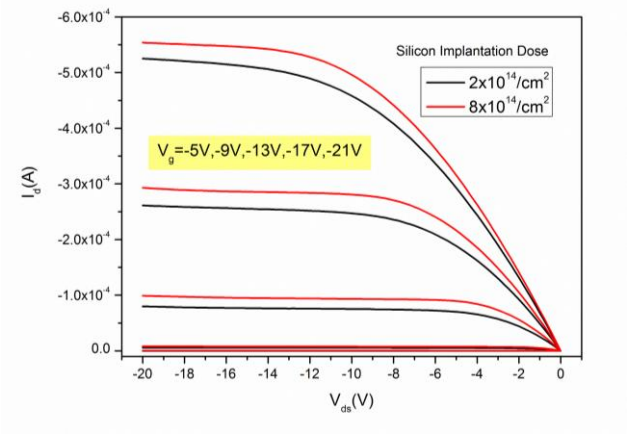
$$\mu_{FE} = \frac{LG_m}{WC_{ox}V_{ds}}$$

where G_m is the maximum value of transconductance at V_{ds}=-0.1 V, C_{ox} is gate oxide capacitance per unit area.

The BG MIC TFTs with silicon implantation dose of 8×10^{14} /cm^2 exhibits larger on-state current, lower leakage current, and higher on-off current ratio. The extracted field-effect mobility is about 109 cm^2/Vs, threshold voltage is 6.4 V, subthreshold swing is 0.8 V/decade, on/off current ratio reaches 4×10^7. The enhanced mobility of TFTs is attributed to the silicon interstitials injected in the poly-Si thin film during the silicon implantation process. These interstitials are incorporated in the grain boundaries, which reduce the defect density and lower the potential barrier at the grain boundaries. The mobility of the poly-Si thin film increase and the devices fabricated on the resulting poly-Si thin film showed better electrical performance.



(a)



(b)

Fig.2. (a) the transfer characteristics and (b) the output characteristics of the proposed TFT.

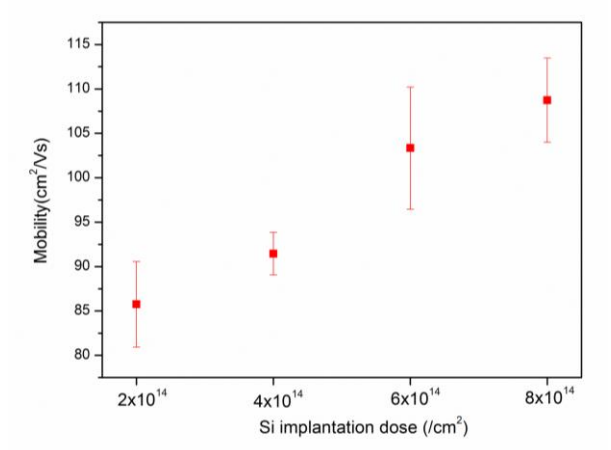


Fig. 3 Field-effect mobility versus silicon implantation dose.

4. Conclusion

The effect of Si self-implantation at non-amorphizing dose is studied. It is shown that the BG MIC TFTs fabricated on the resulting poly-Si thin film exhibit better electrical performance. The BG MIC TFTs with silicon implantation dose of 8×10^{14} /cm^2 have field-effect mobility of 109 cm^2/Vs, threshold voltage of 6.4 V, subthreshold swing of 0.8 V/decade, and on/off current ratio of 4×10^7. The improvement of mobility is attributed to the reduced defect density in the grain boundaries, due to the immigration of silicon self-interstitials to the grain boundaries.

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